# Z0103NA0

## 4Q Triac

4 April 2014 **Product data sheet**

## 1. General description

Planar passivated very sensitive gate four quadrant triac in a SOT54 (TO-92) plastic package intended for use in applications requiring enhanced noise immunity and direct interfacing to logic ICs and low power gate drivers.

## 2. Features and benefits

- Direct interfacing to logic level ICs
- Enhanced current surge capability
- Enhanced noise immunity
- High blocking voltage capability
- Planar passivated for voltage ruggedness and reliability
- Triggering in all four quadrants
- Very sensitive gate in four quadrants

## 3. Applications

- General purpose low power motor control
- Home appliances
- Industrial process control
- Low power AC Fan controllers

## 4. Quick reference data

**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DRM}$ | repetitive peak off-state voltage | | | - | - | 800 | V |
| $I_{TSM}$ | non-repetitive peak on-state current | full sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 20 ms; Fig. 4; Fig. 5 | | - | - | 12.5 | A |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{lead} \leq$ 45 °C; Fig. 1; Fig. 2; Fig. 3 | | - | - | 1 | A |
| **Static characteristics** | | | | | | | |
| $I_{GT}$ | gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A; T2+ G+; $T_j$ = 25 °C; Fig. 7 | | 0.2 | - | 3 | mA |
| | | $V_D$ = 12 V; $I_T$ = 0.1 A; T2+ G-; $T_j$ = 25 °C; Fig. 7 | | 0.2 | - | 3 | mA |

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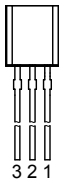
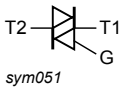
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| | | $V_D$ = 12 V; $I_T$ = 0.1 A; T2- G-; $T_j$ = 25 °C; Fig. 7 | | 0.2 | - | 3 | mA |
| | | $V_D$ = 12 V; $I_T$ = 0.1 A; T2- G+; $T_j$ = 25 °C; Fig. 7 | | 0.2 | - | 5 | mA |

## 5. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | T2 | main terminal 2 |   **TO-92 (SOT54)** |   *sym051* |
| 2 | G | gate | | |
| 3 | T1 | main terminal 1 | | |

## 6. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| Z0103NA0 | TO-92 | plastic single-ended leaded (through hole) package; 3 leads | SOT54 |

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DRM}$ | repetitive peak off-state voltage | | | - | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{lead}$ ≤ 45 °C; Fig. 1; Fig. 2; Fig. 3 | | - | 1 | A |
| $I_{TSM}$ | non-repetitive peak on-state current | full sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 20 ms; Fig. 4; Fig. 5 | | - | 12.5 | A |
| | | full sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 16.7 ms | | - | 13.8 | A |
| $I^2t$ | $I^2t$ for fusing | $t_p$ = 10 ms; SIN | | - | 0.78 | $A^2s$ |
| $dI_T/dt$ | rate of rise of on-state current | $I_T$ = 1 A; $I_G$ = 20 mA; $dI_G/dt$ = 100 mA/µs; T2+ G+ | | - | 50 | A/µs |
| | | $I_T$ = 1 A; $I_G$ = 20 mA; $dI_G/dt$ = 100 mA/µs; T2+ G- | | - | 50 | A/µs |

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| | | $I_T$ = 1 A; $I_G$ = 20 mA; $dI_G/dt$ = 100 mA/µs; T2- G- | | - | 50 | A/µs |
| | | $I_T$ = 1 A; $I_G$ = 20 mA; $dI_G/dt$ = 100 mA/µs; T2- G+ | | - | 20 | A/µs |
| $I_{GM}$ | peak gate current | | | - | 1 | A |
| $P_{GM}$ | peak gate power | | | - | 2 | W |
| $P_{G(AV)}$ | average gate power | over any 20 ms period | | - | 0.1 | W |
| $T_{stg}$ | storage temperature | | | -40 | 150 | °C |
| $T_j$ | junction temperature | | | - | 125 | °C |

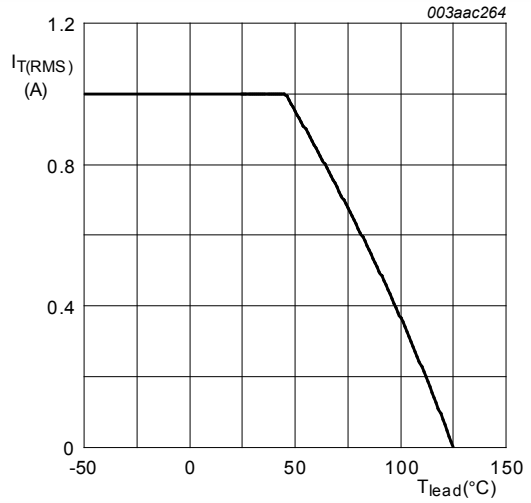
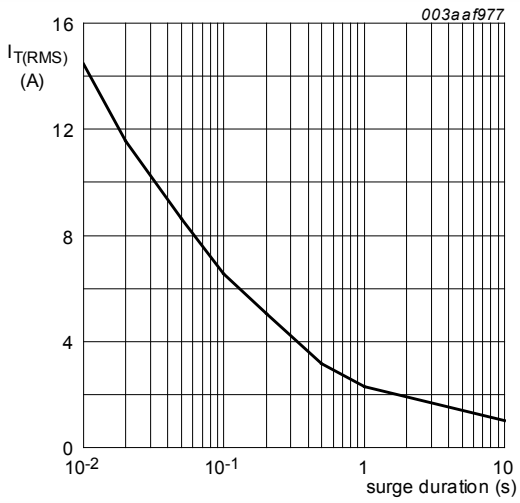
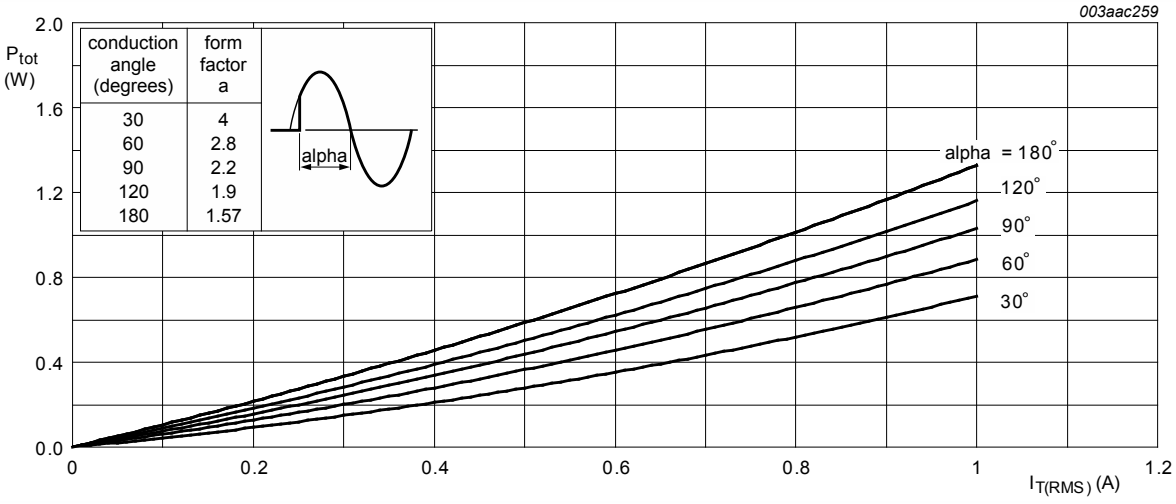



**Fig. 1. RMS on-state current as a function of lead temperature; maximum values**



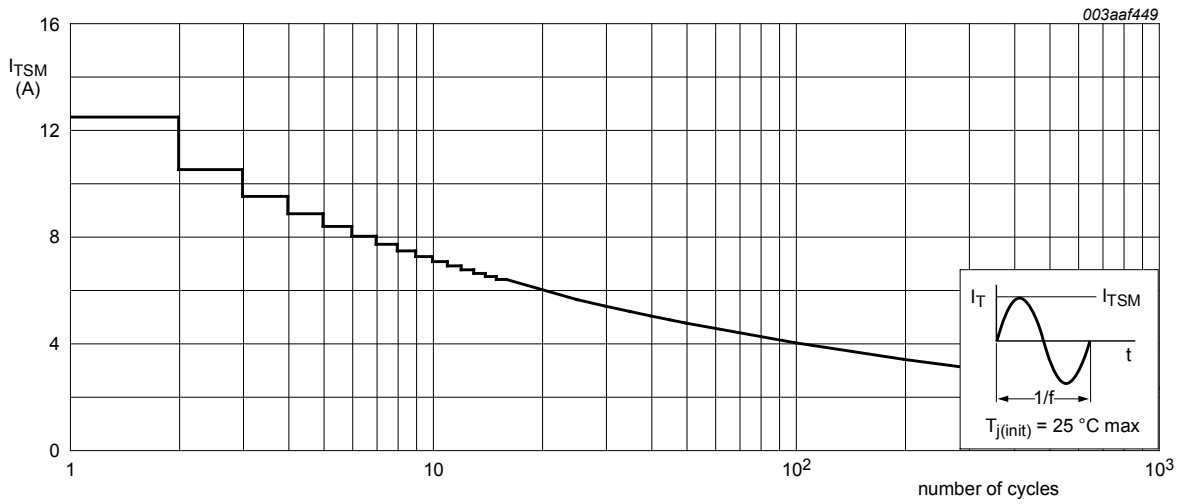

f = 50 Hz; $T_{lead}$ = 45 °C

**Fig. 2. RMS on-state current as a function of surge duration; maximum values**



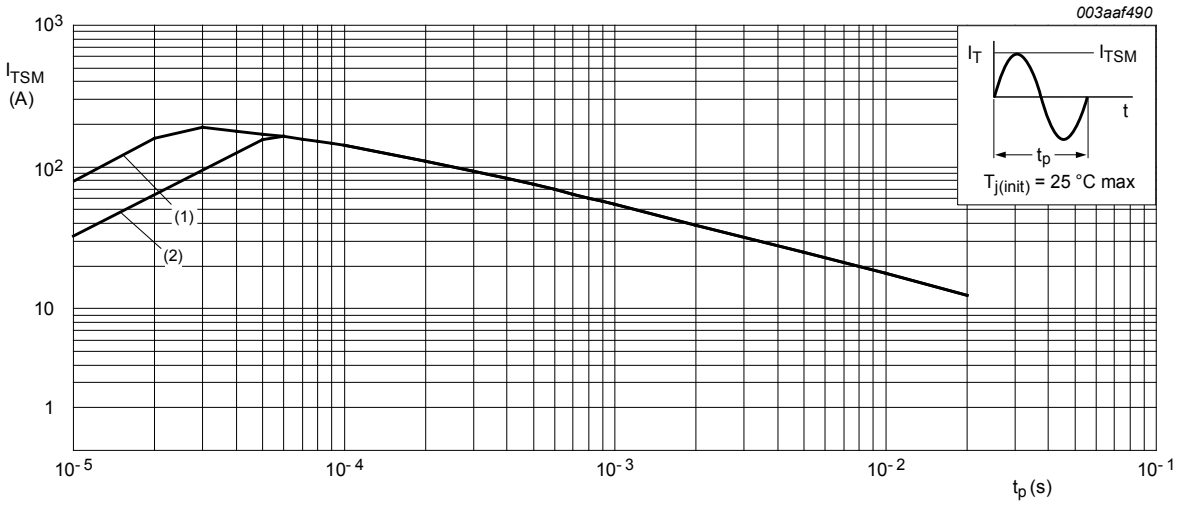

alpha = conduction angle

**Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values**




f = 50 Hz

**Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values**




$t_p \leq 20$ ms

(1) $dI_T/dt$ limit

(2) T2- G+ quadrant limit

**Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values**

# 8. Thermal characteristics

**Table 5. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j\text{-}lead)}$ | thermal resistance from junction to lead | full cycle; Fig. 6 | | - | - | 60 | K/W |
| $R_{th(j\text{-}a)}$ | thermal resistance from junction to ambient | full cycle; printed circuit board mounted; lead length 4 mm | | - | 150 | - | K/W |

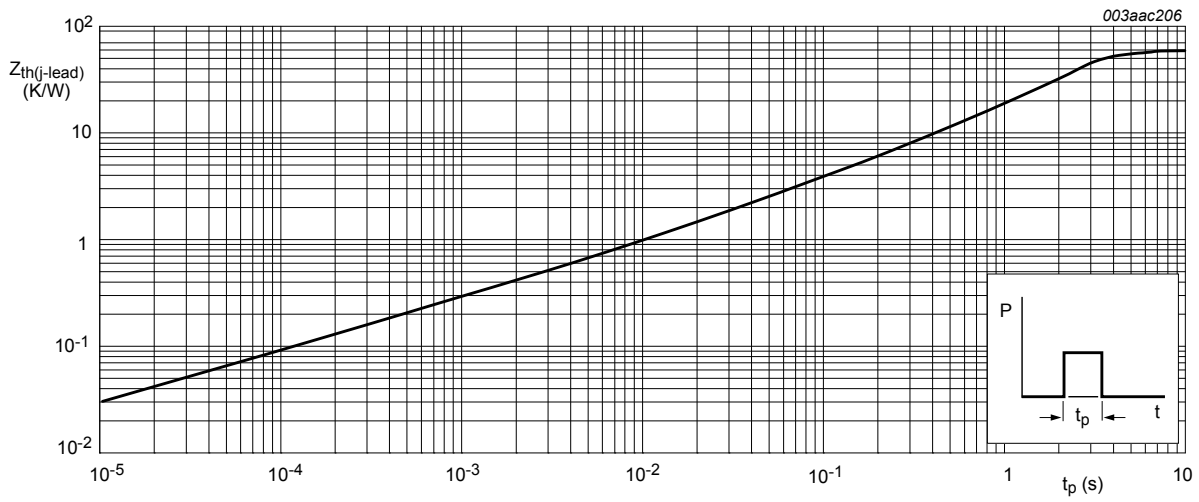


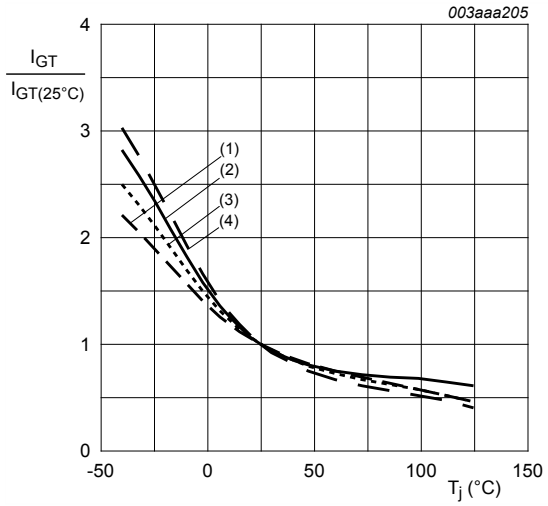

**Fig. 6. Transient thermal impedance from junction to lead as a function of pulse width**

# 9. Characteristics

**Table 6. Characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | | |
| $I_{GT}$ | gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A; T2+ G+; $T_j$ = 25 °C; Fig. 7 | | 0.2 | - | 3 | mA |
| | | $V_D$ = 12 V; $I_T$ = 0.1 A; T2+ G-; $T_j$ = 25 °C; Fig. 7 | | 0.2 | - | 3 | mA |
| | | $V_D$ = 12 V; $I_T$ = 0.1 A; T2- G-; $T_j$ = 25 °C; Fig. 7 | | 0.2 | - | 3 | mA |
| | | $V_D$ = 12 V; $I_T$ = 0.1 A; T2- G+; $T_j$ = 25 °C; Fig. 7 | | 0.2 | - | 5 | mA |
| $I_L$ | latching current | $V_D$ = 12 V; $I_G$ = 0.1 A; T2+ G+; $T_j$ = 25 °C; Fig. 8 | | - | - | 7 | mA |
| | | $V_D$ = 12 V; $I_G$ = 0.1 A; T2+ G-; $T_j$ = 25 °C; Fig. 8 | | - | - | 20 | mA |
| | | $V_D$ = 12 V; $I_G$ = 0.1 A; T2- G-; $T_j$ = 25 °C; Fig. 8 | | - | - | 7 | mA |
| | | $V_D$ = 12 V; $I_G$ = 0.1 A; T2- G+; $T_j$ = 25 °C; Fig. 8 | | - | - | 7 | mA |
| $I_H$ | holding current | $V_D$ = 12 V; $T_j$ = 25 °C; Fig. 9 | | - | - | 7 | mA |
| $V_T$ | on-state voltage | $I_T$ = 1 A; $T_j$ = 25 °C; Fig. 10 | | - | 1.3 | 1.6 | V |
| $V_{GT}$ | gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A; $T_j$ = 25 °C; Fig. 11 | | - | - | 1 | V |

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| | | $V_D$ = 800 V; $I_T$ = 0.1 A; $T_j$ = 125 °C; Fig. 11 | | 0.2 | - | - | V |
| $I_D$ | off-state current | $V_D$ = 800 V; $T_j$ = 125 °C | | - | - | 0.5 | mA |
| **Dynamic characteristics** | | | | | | | |
| $dV_D/dt$ | rate of rise of off-state voltage | $V_{DM}$ = 536 V; $T_j$ = 110 °C; ($V_{DM}$ = 67% of $V_{DRM}$); exponential waveform; gate open circuit; Fig. 12 | | 80 | - | - | V/µs |
| $dV_{com}/dt$ | rate of change of commutating voltage | $V_D$ = 400 V; $T_j$ = 110 °C; $dI_{com}/dt$ = 0.44 A/ms; gate open circuit | | 0.5 | - | - | V/µs |




(1) T2- G+
(2) T2- G-
(3) T2+ G-
(4) T2+ G+

**Fig. 7. Normalized gate trigger current as a function of junction temperature**

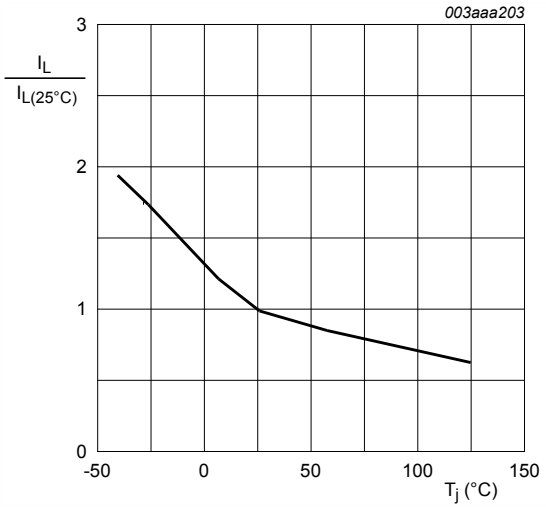



**Fig. 8. Normalized latching current as a function of junction temperature**

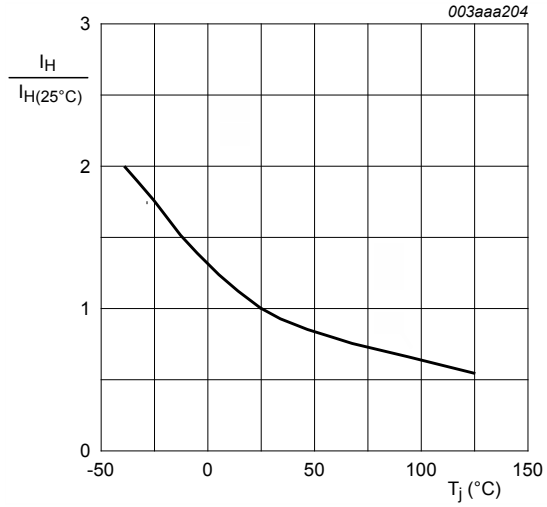
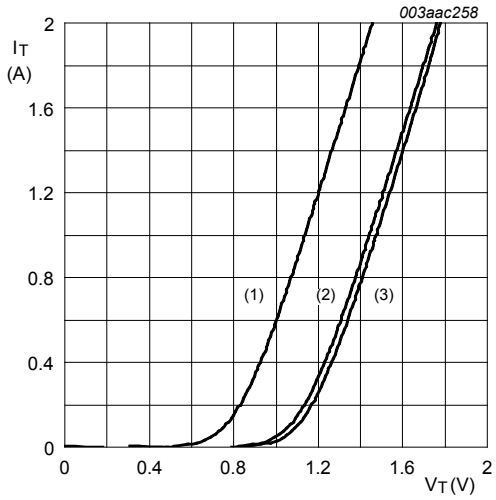



**Fig. 9. Normalized holding current as a function of junction temperature**




$V_o$ = 1.13 V

$R_s$ = 0.31 Ω

(1) $T_j$ = 125 °C; typical values

(2) $T_j$ = 125 °C; maximum values

(3) $T_j$ = 25 °C; maximum values

**Fig. 10. On-state current as a function of on-state voltage**

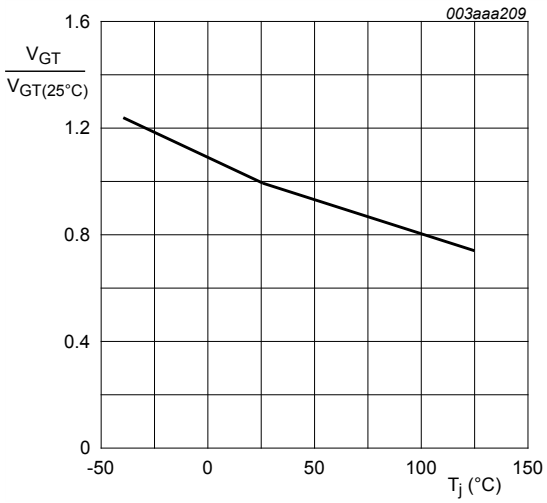



**Fig. 11. Normalized gate trigger voltage as a function of junction temperature**

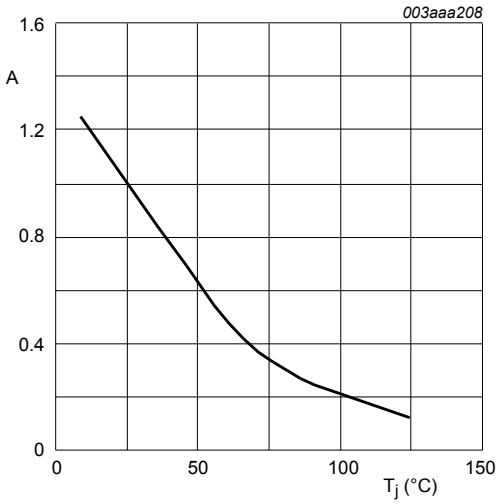
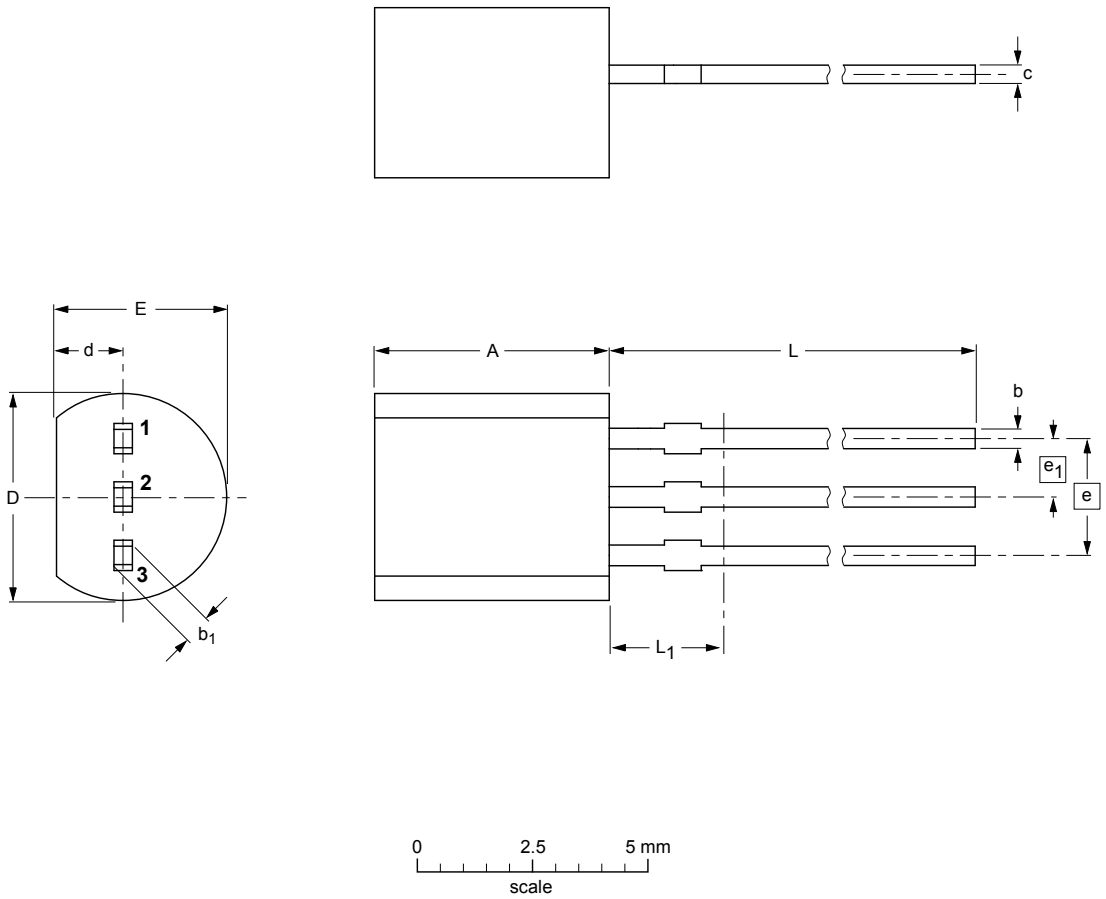



**Fig. 12. Normalized critical rate of rise of off-state voltage as a function of junction temperature; typical values**

$$A = \frac{dV_{D(Tj\,°C)} / dt}{dV_{D(25\,°C)} / dt}$$

## 10. Package outline

**Plastic single-ended leaded (through hole) package; 3 leads** **SOT54**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | b | $b_1$ | c | D | d | E | e | $e_1$ | L | $L_1$ (1) max. |
|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 5.2<br>5.0 | 0.48<br>0.40 | 0.66<br>0.55 | 0.45<br>0.38 | 4.8<br>4.4 | 1.7<br>1.4 | 4.2<br>3.6 | 2.54 | 1.27 | 14.5<br>12.7 | 2.5 |

**Note**

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT54 | | TO-92 | SC-43A | | | ~~04-06-28~~<br>04-11-16 |

**Fig. 13. Package outline TO-92 (SOT54)**

# 11. Legal information

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| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
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