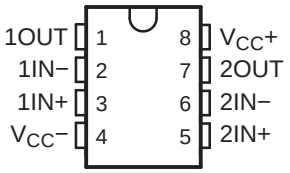
DUAL GENERAL-PURPOSE OPERATIONAL AMPLIFIER

Check for Samples: RC4558

FEATURES

- **Continuous Short-Circuit Protection**
- **Wide Common-Mode and Differential Voltage Ranges**
- **No Frequency Compensation Required**
- **Low Power Consumption**
- **No Latch-Up**
- **Unity-Gain Bandwidth . . . 3 MHz Typ**
- **Gain and Phase Match Between Amplifiers**
- **Low Noise . . . 8 nV/$\sqrt{Hz}$ Typ at 1 kHz**

D, DGK, P, PS, OR PW PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The RC4558 device is a dual general-purpose operational amplifier, with each half electrically similar to the µA741, except that offset null capability is not provided.

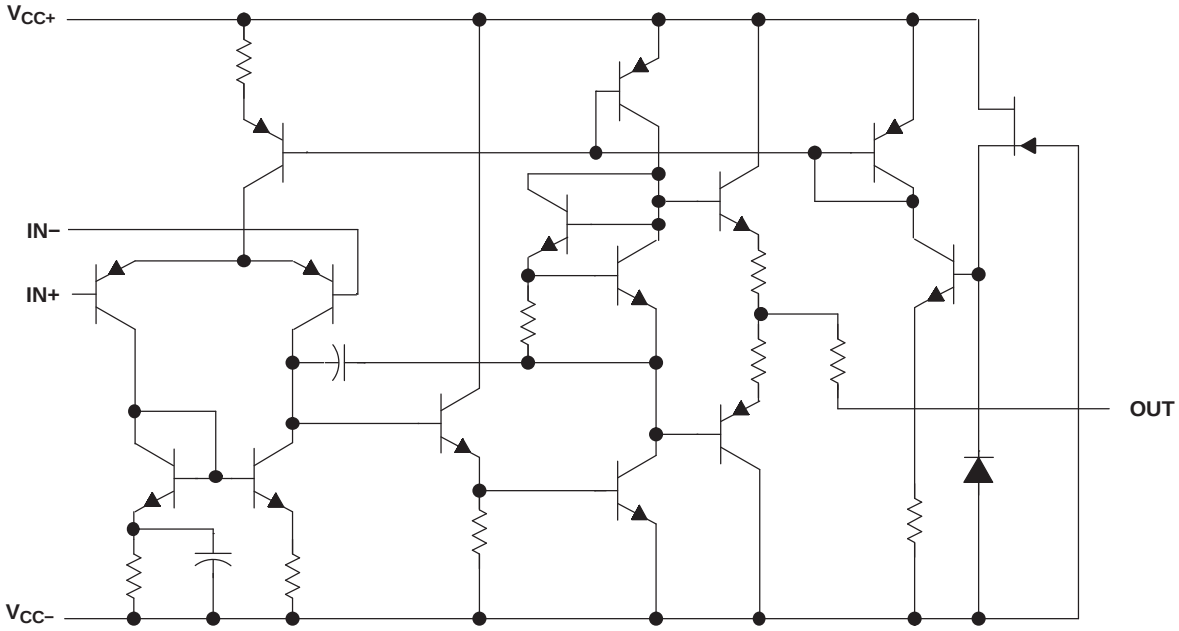
The high common-mode input voltage range and the absence of latch-up make this amplifier ideal for voltage-follower applications. The device is short-circuit protected, and the internal frequency compensation ensures stability without external components.

Table 1. ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	MSOP/VSSOP – DGK	Reel of 2500	RC4558DGKR	YR_(2)
	PDIP – P	Tube of 50	RC4558P	RC4558P
	SOIC – D	Tube of 75	RC4558D	RC4558
		Reel of 2500	RC4558DRG3	
	SOP – PS	Reel of 2000	RC4558PSR	R4558
	TSSOP – PW	Tube of 150	RC4558PW	R4558
		Reel of 2000	RC4558PWR	
–40°C to 85°C	MSOP/VSSOP – DGK	Reel of 2500	RC4558IDGKR	YS_(2)
	PDIP – P	Tube of 50	RC4558IP	RC4558IP
	SOIC – D	Tube of 75	RC4558ID	R4558I
		Reel of 2500	RC4558IDR	
	TSSOP – PW	Tube of 150	RC4558IPW	R4558I
		Reel of 2000	RC4558IPWR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) The actual top-side marking has one additional character that designates the assembly/test site.

SCHEMATIC (EACH AMPLIFIER)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC+}	Supply voltage(2)			18	V
V_{CC-}				–18	
V_{ID}	Differential input voltage(3)			±30	V
V_I	Input voltage (any input)(2) (4)			±15	V
	Duration of output short circuit to ground, one amplifier at a time(5)			Unlimited	
θ_{JA}	Package thermal impedance(6) (7)	D package		97	°C/W
		DGK package		172	
		P package		85	
		PS package		95	
		PW package		149	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
(3) Differential voltages are at IN+ with respect to IN–.
(4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
(5) Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
(6) Maximum power dissipation is a function of T_J (max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J (max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(7) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC+}	Supply voltage		5	15	V
V_{CC-}			–5	–15	
T_A	Operating free-air temperature	RC4558	0	70	°C
		RC4558I	–40	85	

Electrical Characteristics

at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = –15 V

PARAMETER			TEST CONDITIONS(1)	T_A (2)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		V_O = 0	25°C		0.5	6	mV
				Full range			7.5	
I_{IO}	Input offset current		V_O = 0	25°C		5	200	nA
				Full range			300	
I_{IB}	Input bias current		V_O = 0	25°C		150	500	nA
				Full range			800	
V_{ICR}	Common-mode input voltage range			25°C	±12	±14		V
V_{OM}	Maximum output voltage swing		R_L = 10 kΩ	25°C	±12	±14		V
			R_L = 2 kΩ	25°C	±10	±13		
				Full range	±10			
A_{VD}	Large-signal differential voltage amplification		R_L ≥ 2 kΩ, V_O = ±10 V	25°C	20	300		V/mV
				Full range	15			
B_1	Unity-gain bandwith			25°C		3		MHz
r_i	Input resistance			25°C	0.3	5		MΩ
CMRR	Common-mode rejection ratio			25°C	70	90		dB
k_{SVS}	Supply-voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)		V_{CC} = ±15 V to ±9 V	25°C		30	150	μV/V
V_n	Equivalent input noise voltage (closed loop)		A_{VD} = 100, R_S = 100 Ω, f = 1 kHz, BW = 1 Hz	25°C		8		nV/√Hz
I_{CC}	Supply current (both amplifiers)		V_O = 0, No load	25°C		2.5	5.6	mA
				T_A min		3	6.6	
				T_A max		2.3	5	
P_D	Total power dissipation (both amplifiers)		V_O = 0, No load	25°C		75	170	mW
				T_A min		90	200	
				T_A max		70	150	
V_{O1}/V_{O2}	Crosstalk attenuation	Open loop	R_S = 1 kΩ, f = 10 kHz	25°C		85		dB
		A_{VD} = 100				105		

(1) All characteristics are measured under open-loop conditions with zero common-mode input voltage, unless otherwise specified.
(2) Full range is 0°C to 70°C for RC4558 and –40°C to 85°C for RC4558I.

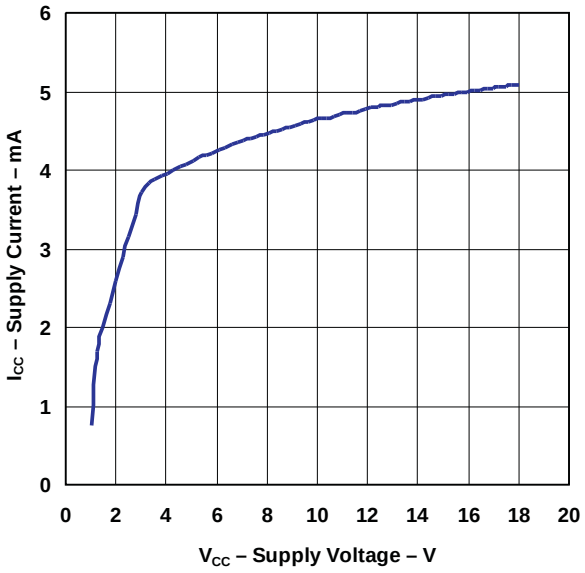
Operating Characteristics

V_{CC+} = 15 V, V_{CC-} = –15 V, T_A = 25°C

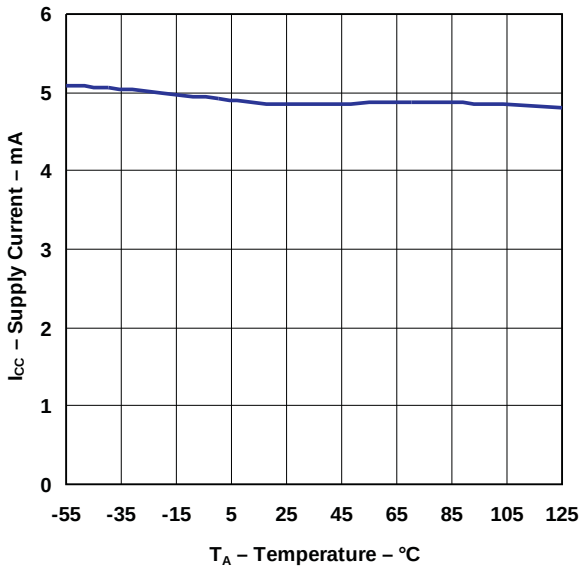
PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_r	Rise time	V_I = 20 mV,	R_L = 2 kΩ,	C_L = 100 pF		0.13		ns
	Overshoot	V_I = 20 mV,	R_L = 2 kΩ,	C_L = 100 pF		5		%
SR	Slew rate at unity gain	V_I = 10 V,	R_L = 2 kΩ,	C_L = 100 pF	1.1	1.7		V/μs

TYPICAL CHARACTERISTICS

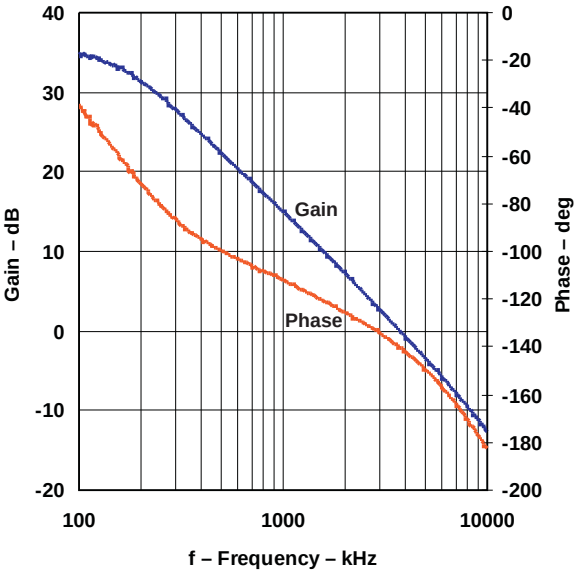
SUPPLY CURRENT vs SUPPLY VOLTAGE (T_A = 25°C)



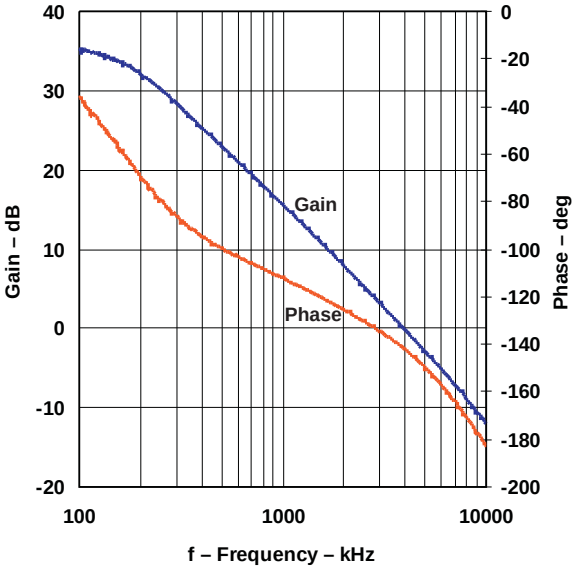
SUPPLY CURRENT vs TEMPERATURE (V_{CC} = ±15 V)



GAIN AND PHASE vs FREQUENCY (V_{CC} = ±15 V, R_L = 2 kΩ, C_L = 22 pF)

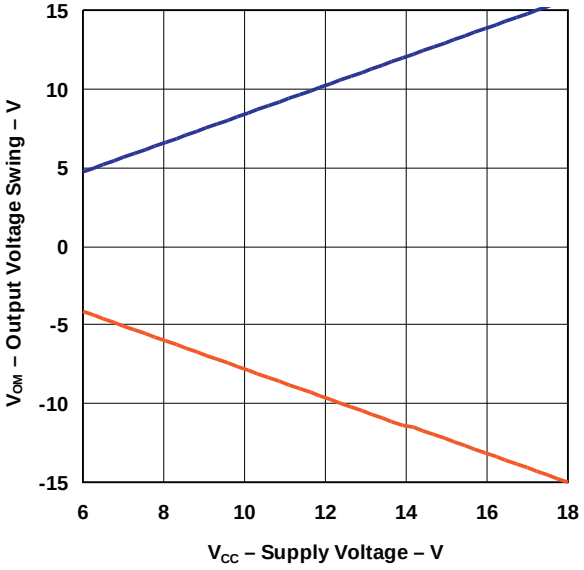


GAIN AND PHASE vs FREQUENCY (V_{CC} = ±15 V, R_L = 10 kΩ, C_L = 22 pF)

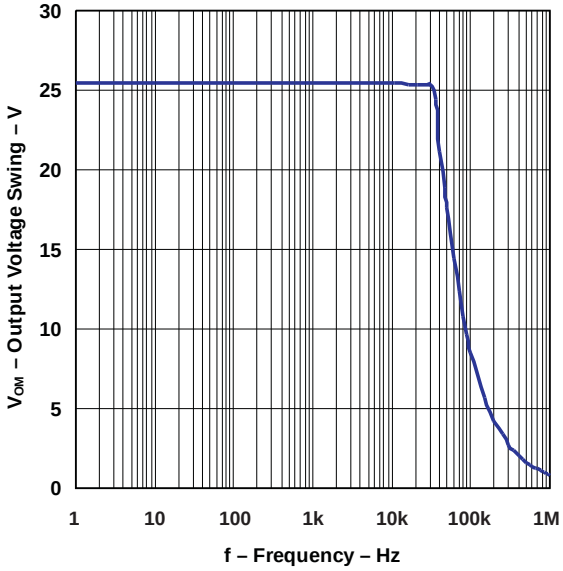


TYPICAL CHARACTERISTICS (continued)

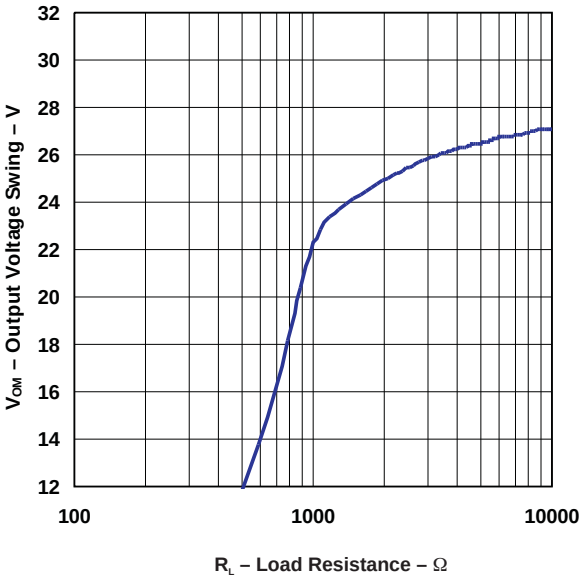
OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE (R_L = 2 kΩ, T_A = 25°C)



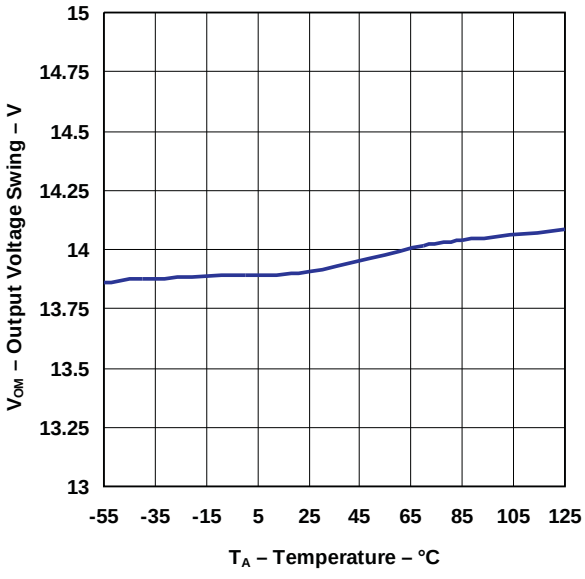
OUTPUT VOLTAGE SWING vs FREQUENCY (V_{CC} = ±15 V, R_L = 2 kΩ, T_A = 25°C)



OUTPUT VOLTAGE SWING vs LOAD RESISTANCE (V_{CC} = ±15 V, T_A = 25°C)

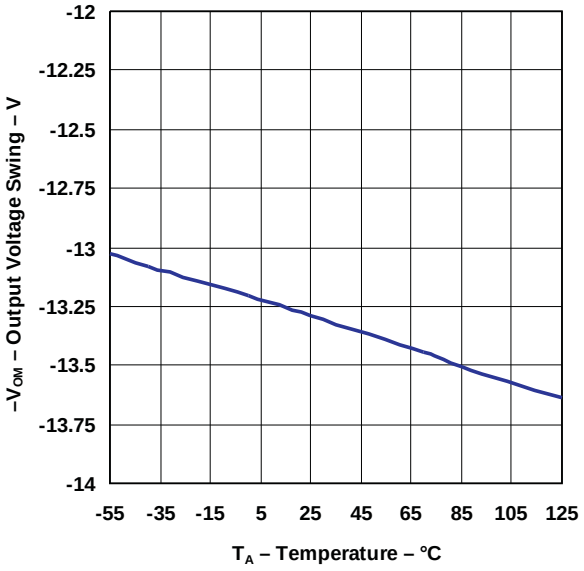


OUTPUT VOLTAGE SWING vs TEMPERATURE (V_{CC} = ±15 V, R_L = 10 kΩ)

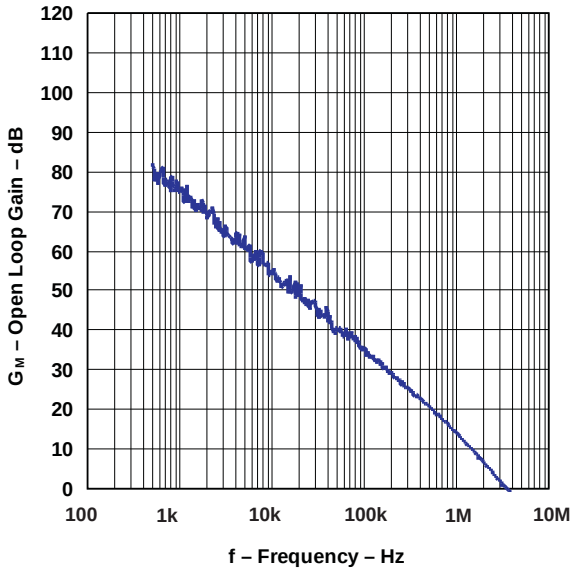


TYPICAL CHARACTERISTICS (continued)

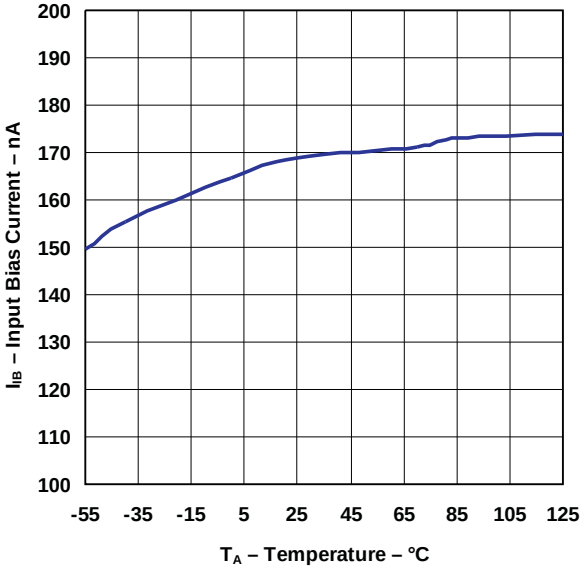
NEGATIVE OUTPUT VOLTAGE SWING vs TEMPERATURE (V_{CC} = ±15 V, R_L = 10 kΩ)



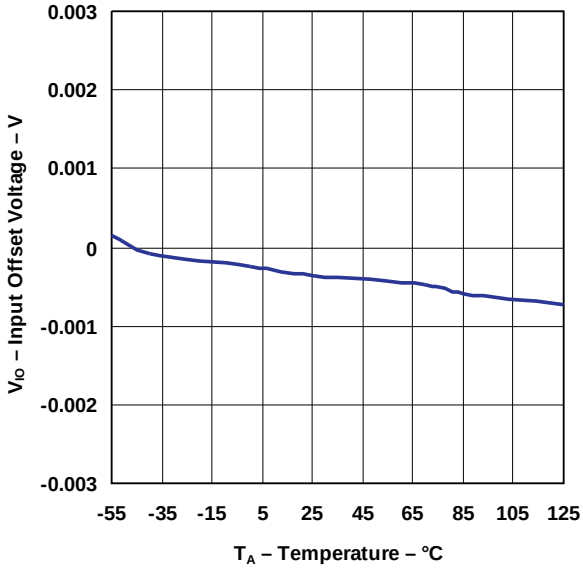
OPEN LOOP GAIN vs FREQUENCY (V_{CC} = ±15 V, R_L = 2 kΩ, C_L = 22 pF, T_A = 25°C)



INPUT BIAS CURRENT vs TEMPERATURE (V_{CC} = ±15 V)

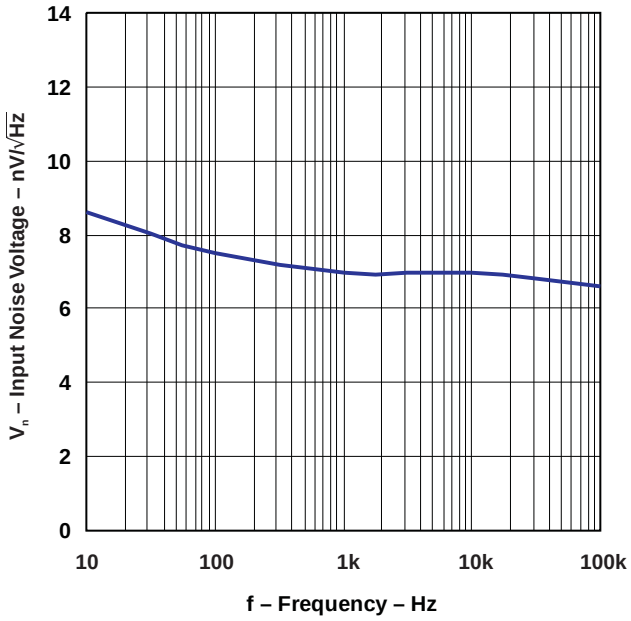


INPUT OFFSET VOLTAGE vs TEMPERATURE (V_{CC} = ±15 V)



TYPICAL CHARACTERISTICS (continued)

INPUT NOISE VOLTAGE
vs
FREQUENCY
(V_{CC} = ±15 V, T_A = 25°C)



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
RC4558-W	ACTIVE	WAFERSALE	YS	0		TBD	Call TI	Call TI			Samples
RC4558D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	RC4558	Samples
RC4558DE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	RC4558	Samples
RC4558DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	RC4558	Samples
RC4558DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(YRP ~ YRS ~ YRU)	Samples
RC4558DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	(YRP ~ YRS ~ YRU)	Samples
RC4558DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	0 to 70	RC4558	Samples
RC4558DRE4	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI	0 to 70		Samples
RC4558DRG3	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	RC4558	Samples
RC4558DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	RC4558	Samples
RC4558ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R4558I	Samples
RC4558IDE4	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85		Samples
RC4558IDG4	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85		Samples
RC4558IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(YSP ~ YSS ~ YSU)	Samples
RC4558IDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(YSP ~ YSS ~ YSU)	Samples
RC4558IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R4558I	Samples
RC4558IDRE4	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85		Samples
RC4558IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R4558I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
RC4558IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	RC4558IP	Samples
RC4558IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	RC4558IP	Samples
RC4558IPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R4558I	Samples
RC4558IPWE4	ACTIVE	TSSOP	PW	8		TBD	Call TI	Call TI	-40 to 85		Samples
RC4558IPWG4	ACTIVE	TSSOP	PW	8		TBD	Call TI	Call TI	-40 to 85		Samples
RC4558IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	R4558I	Samples
RC4558IPWRE4	ACTIVE	TSSOP	PW	8		TBD	Call TI	Call TI	-40 to 85		Samples
RC4558IPWRG4	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	-40 to 85	R4558I	
RC4558P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	RC4558P	Samples
RC4558PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	RC4558P	Samples
RC4558PSLE	OBSOLETE	SO	PS	8		TBD	Call TI	Call TI	0 to 70		
RC4558PSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	R4558	Samples
RC4558PSRE4	ACTIVE	SO	PS	8		TBD	Call TI	Call TI	0 to 70		Samples
RC4558PSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	R4558	Samples
RC4558PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	R4558	Samples
RC4558PWE4	ACTIVE	TSSOP	PW	8		TBD	Call TI	Call TI	0 to 70		Samples
RC4558PWG4	ACTIVE	TSSOP	PW	8		TBD	Call TI	Call TI	0 to 70		Samples
RC4558PWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	0 to 70		
RC4558PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	0 to 70	R4558	Samples
RC4558PWRE4	ACTIVE	TSSOP	PW	8		TBD	Call TI	Call TI	0 to 70		Samples
RC4558PWRG4	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	0 to 70	R4558	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
RC4558Y	OBSOLETE	DIESALE	Y	0		TBD	Call TI	Call TI			

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

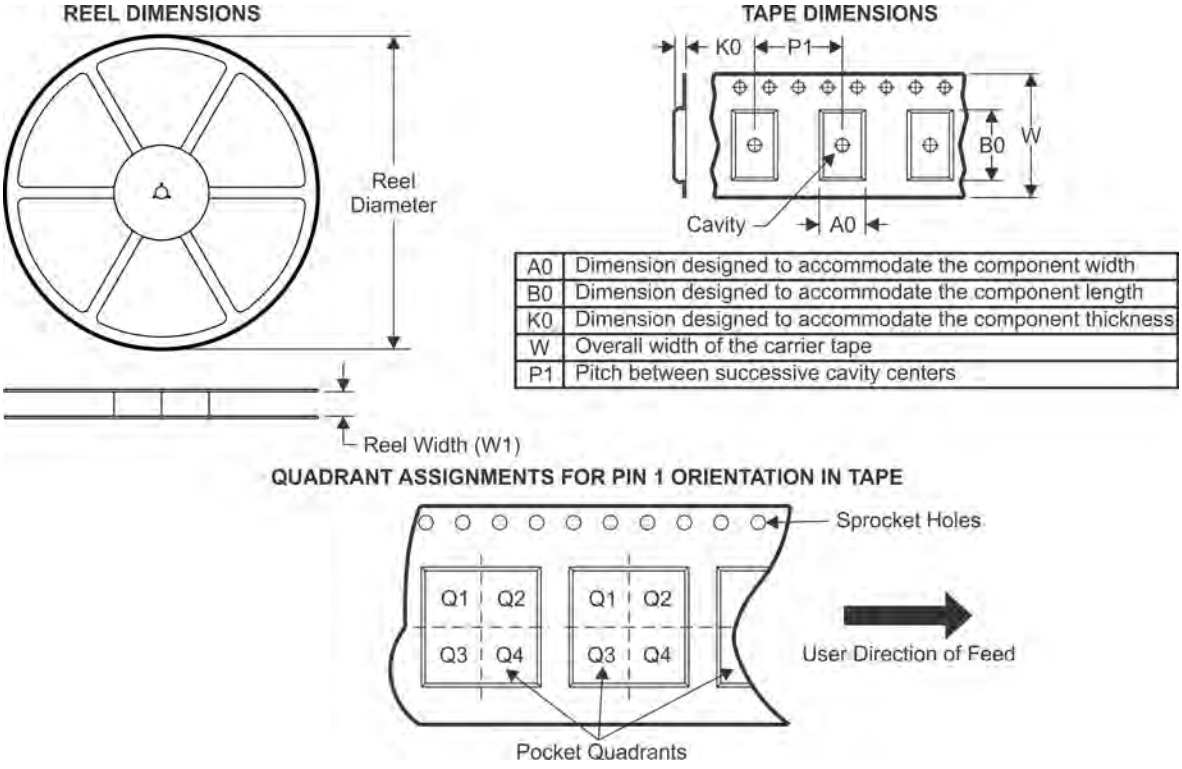
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

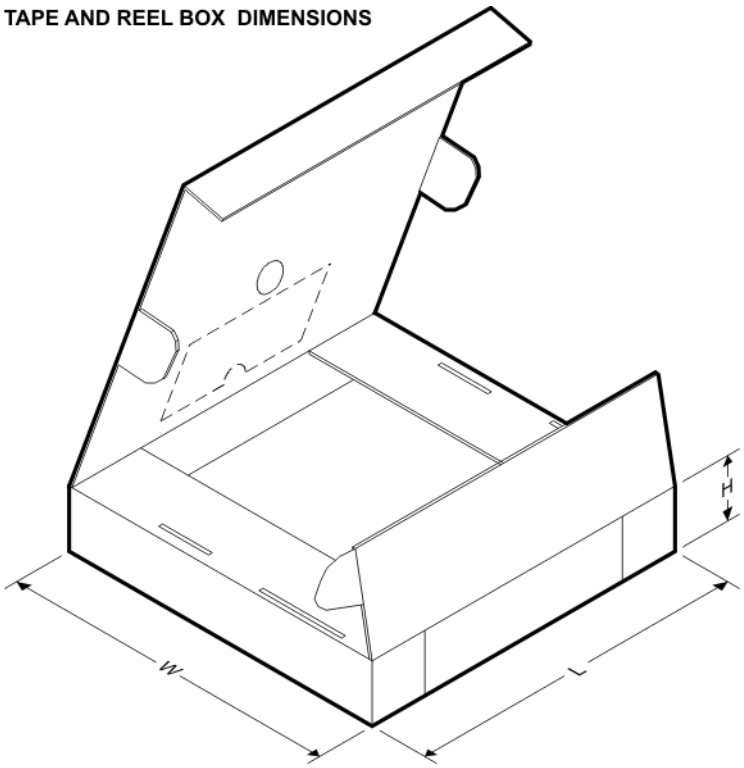


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
RC4558DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
RC4558DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
RC4558DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
RC4558DR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
RC4558DRG3	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
RC4558DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
RC4558DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
RC4558IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
RC4558IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
RC4558IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
RC4558IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
RC4558PSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
RC4558PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

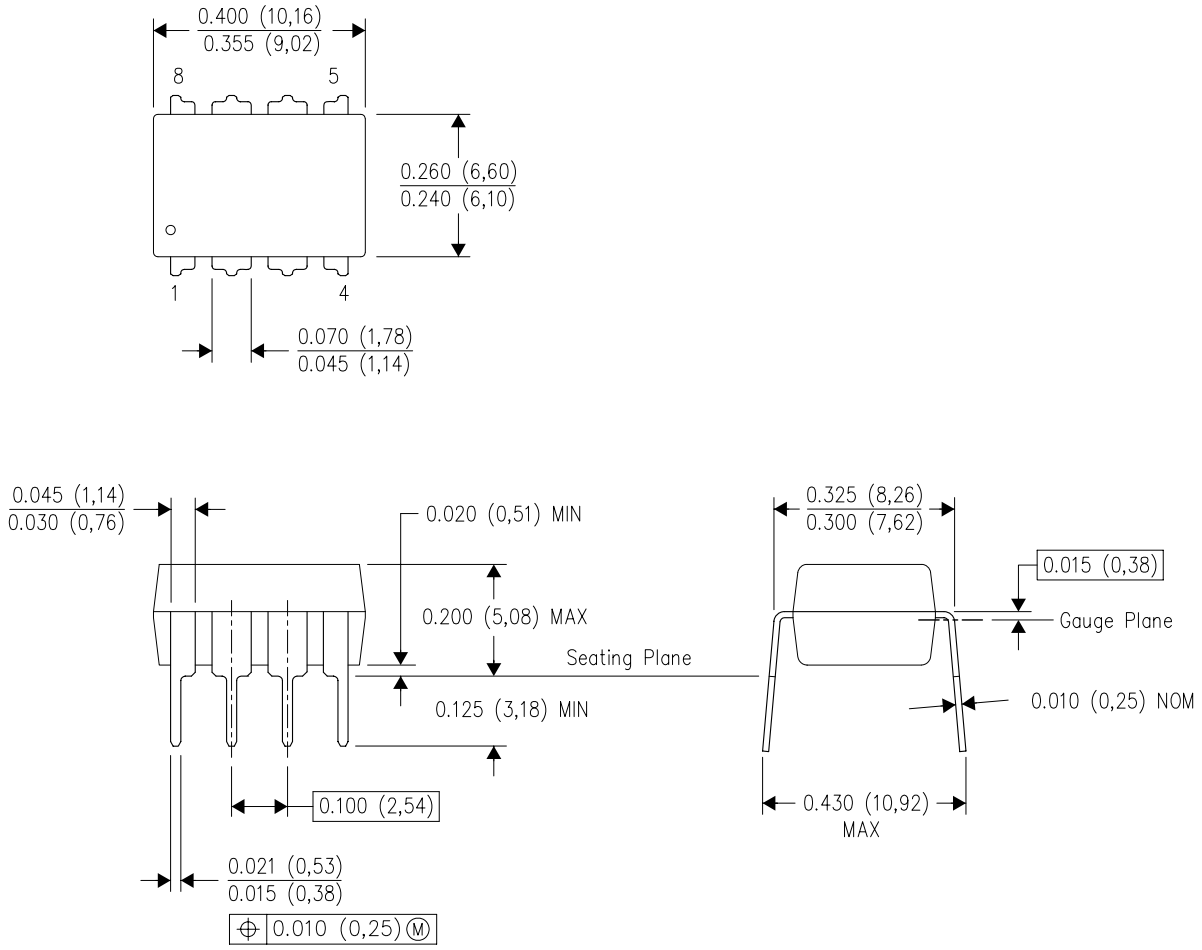
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

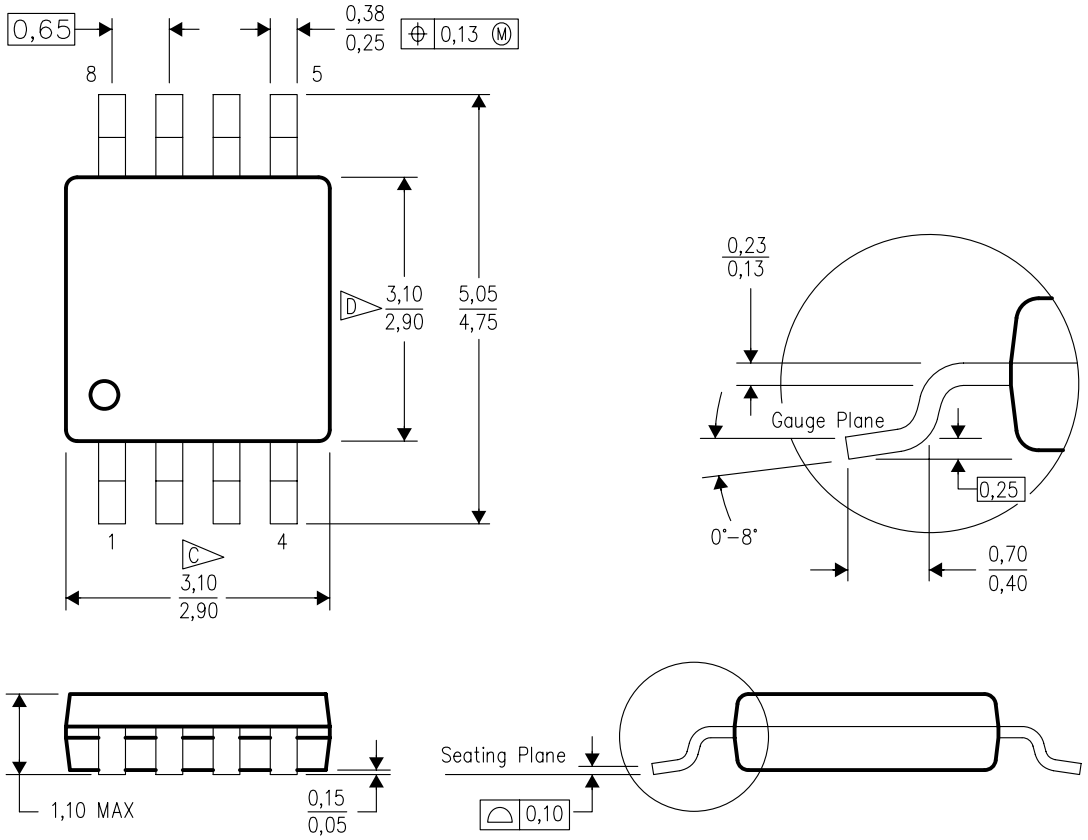
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
RC4558DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
RC4558DR	SOIC	D	8	2500	367.0	367.0	35.0
RC4558DR	SOIC	D	8	2500	340.5	338.1	20.6
RC4558DR	SOIC	D	8	2500	364.0	364.0	27.0
RC4558DRG3	SOIC	D	8	2500	364.0	364.0	27.0
RC4558DRG4	SOIC	D	8	2500	367.0	367.0	35.0
RC4558DRG4	SOIC	D	8	2500	340.5	338.1	20.6
RC4558IDGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
RC4558IDR	SOIC	D	8	2500	340.5	338.1	20.6
RC4558IPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
RC4558IPWR	TSSOP	PW	8	2000	364.0	364.0	27.0
RC4558PSR	SO	PS	8	2000	367.0	367.0	38.0
RC4558PWR	TSSOP	PW	8	2000	364.0	364.0	27.0

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

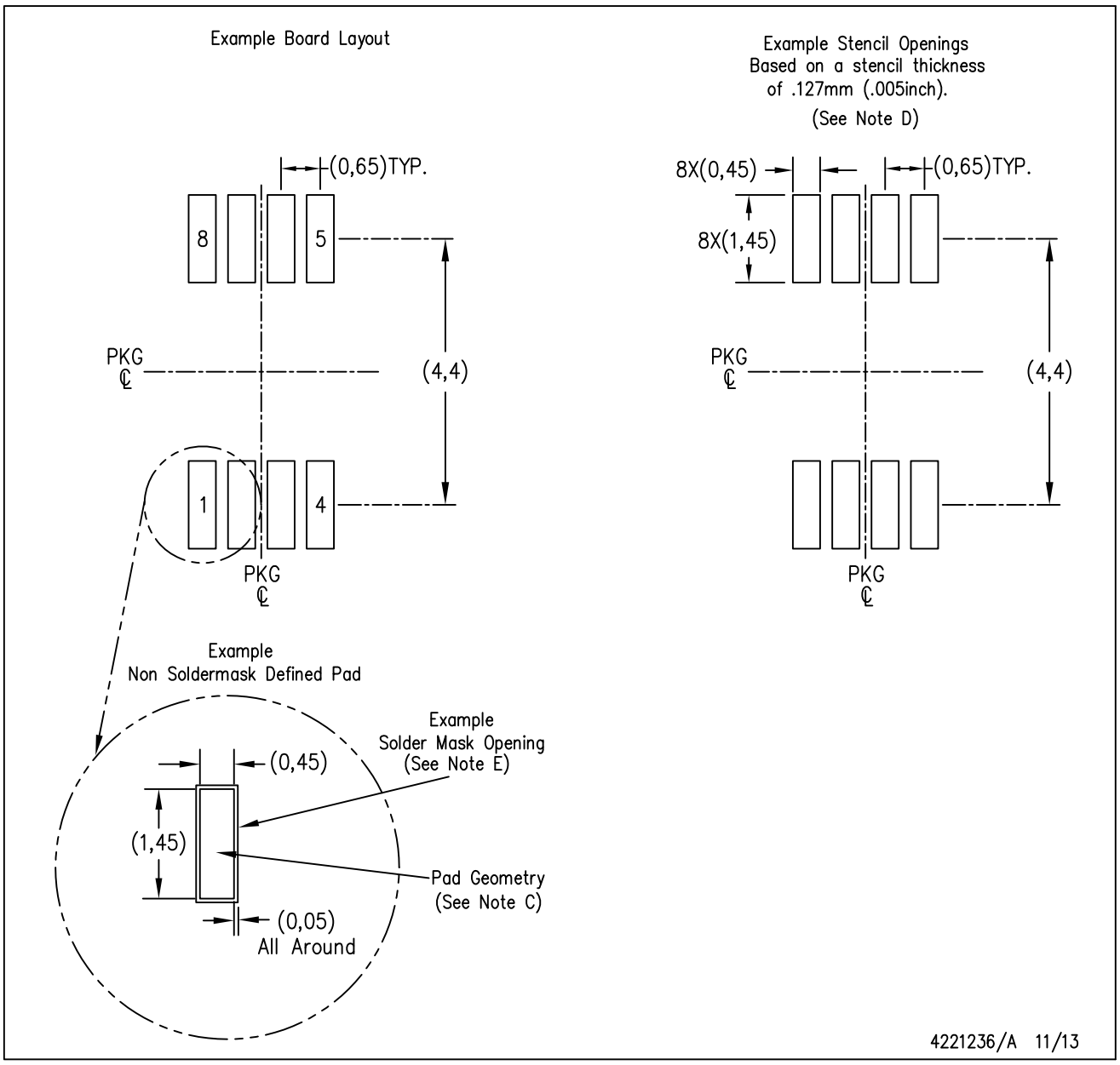
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

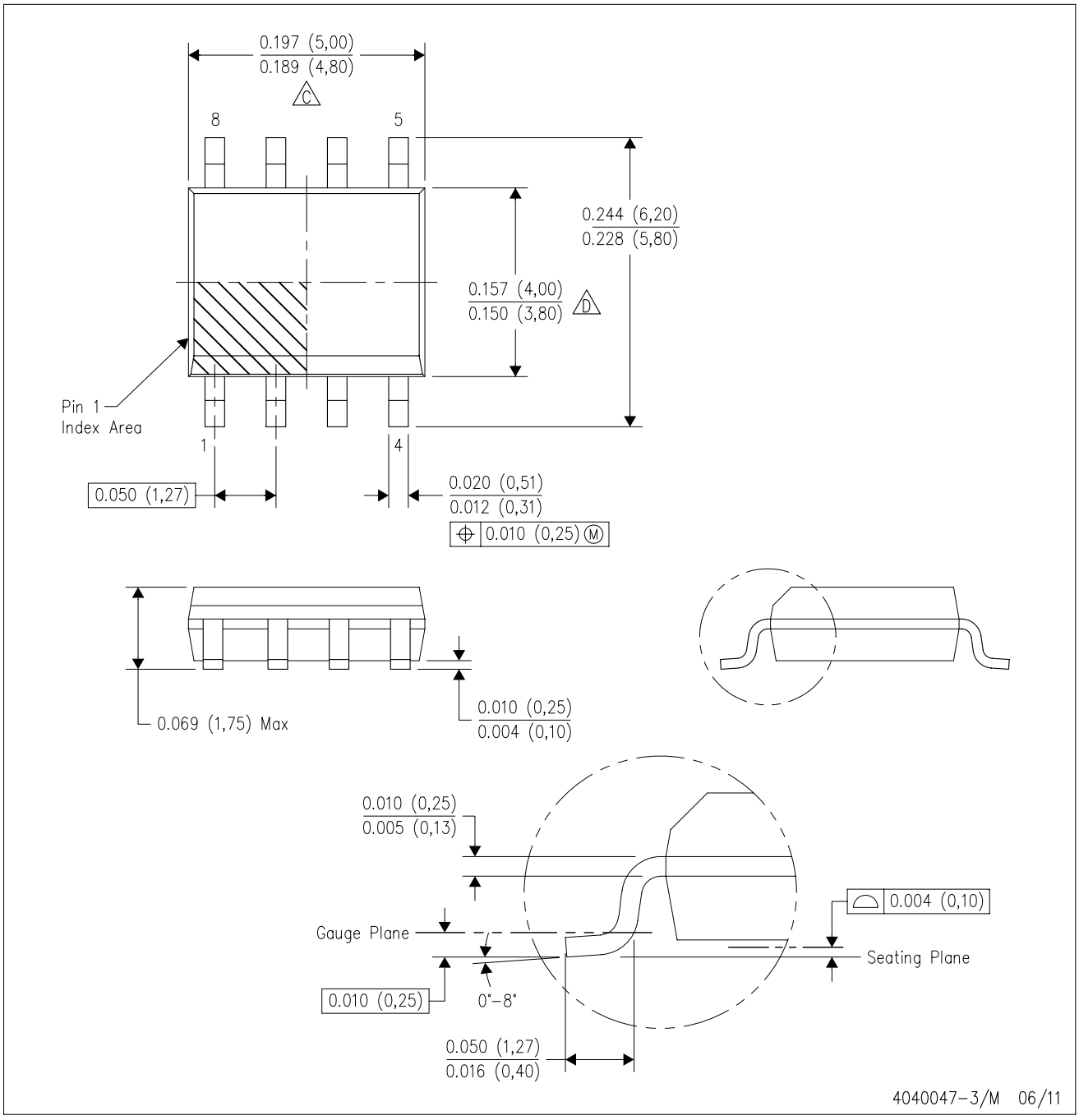
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



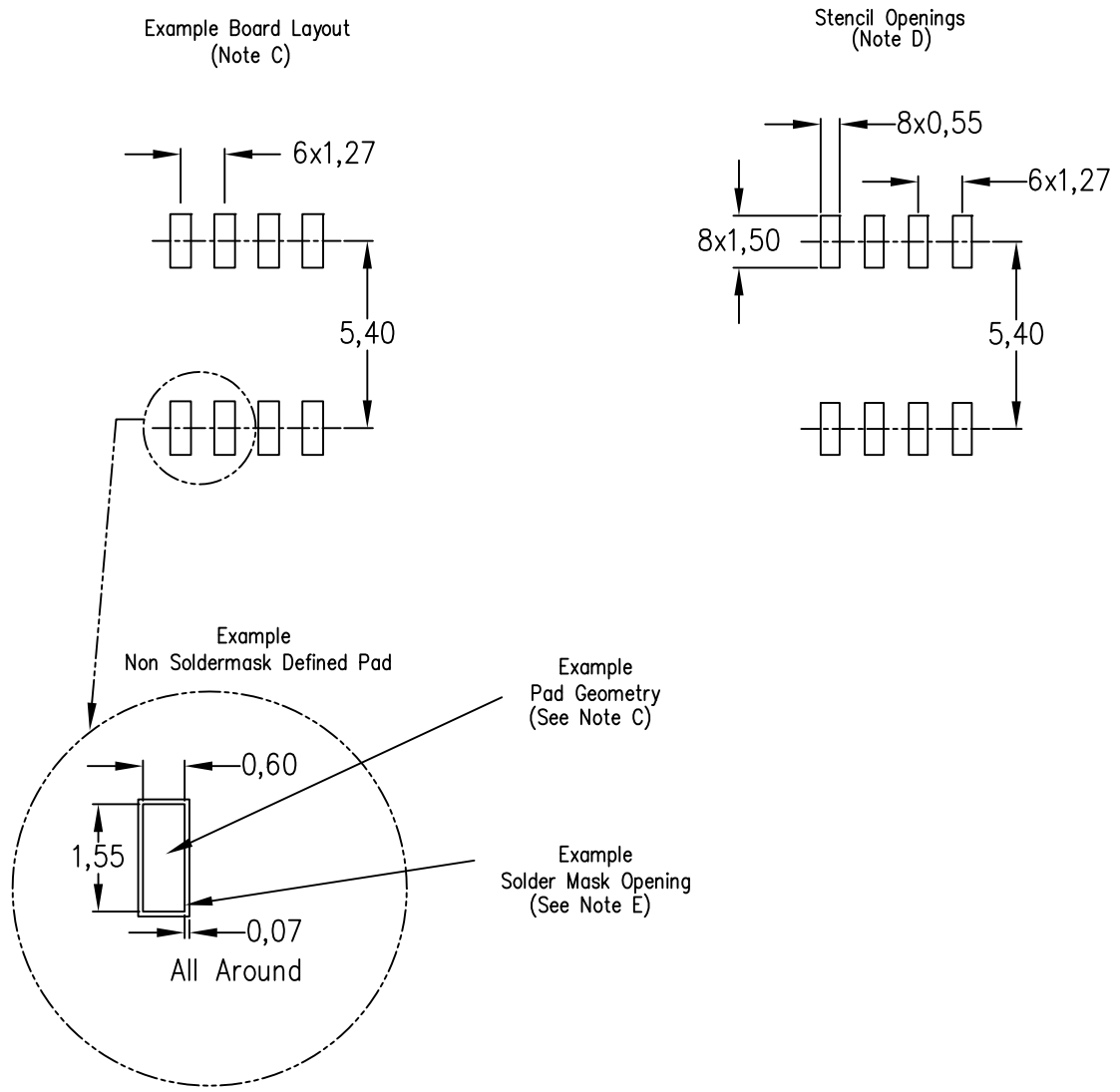
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

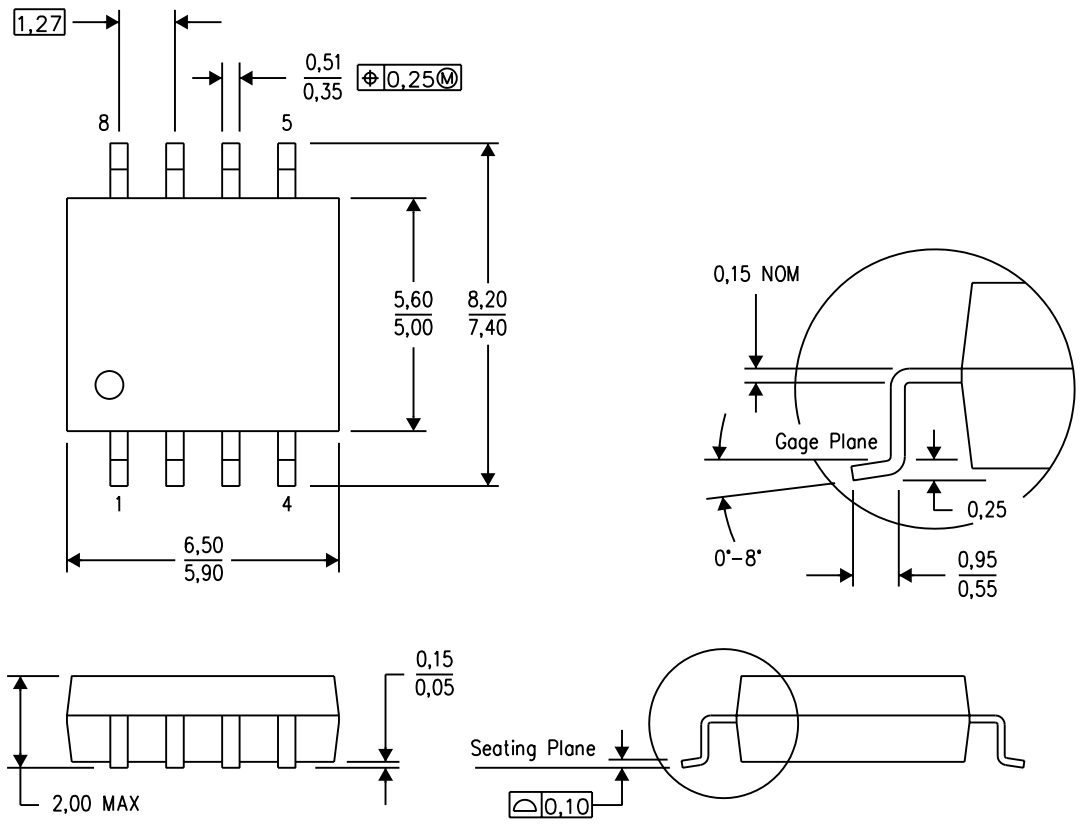
D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

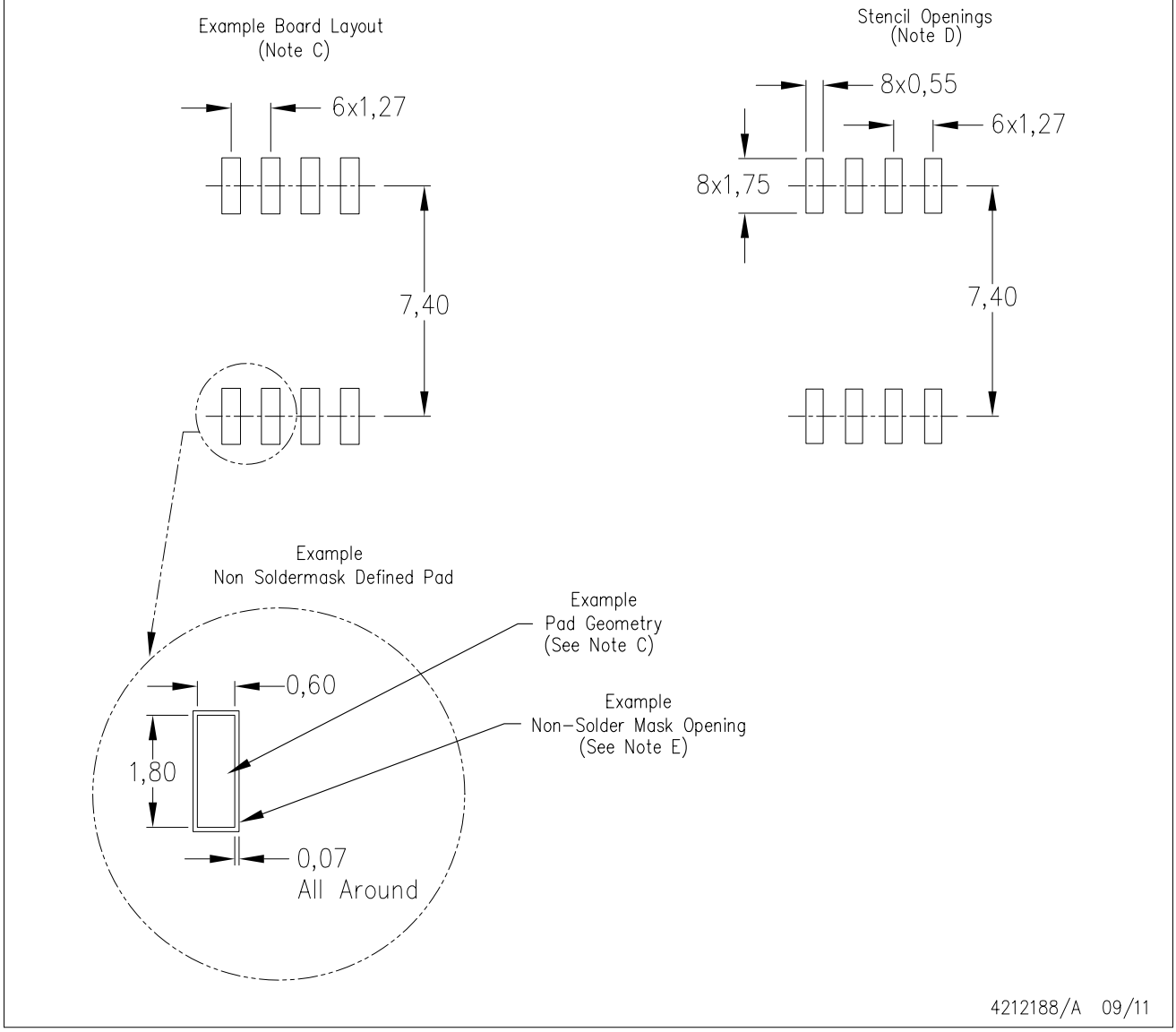
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

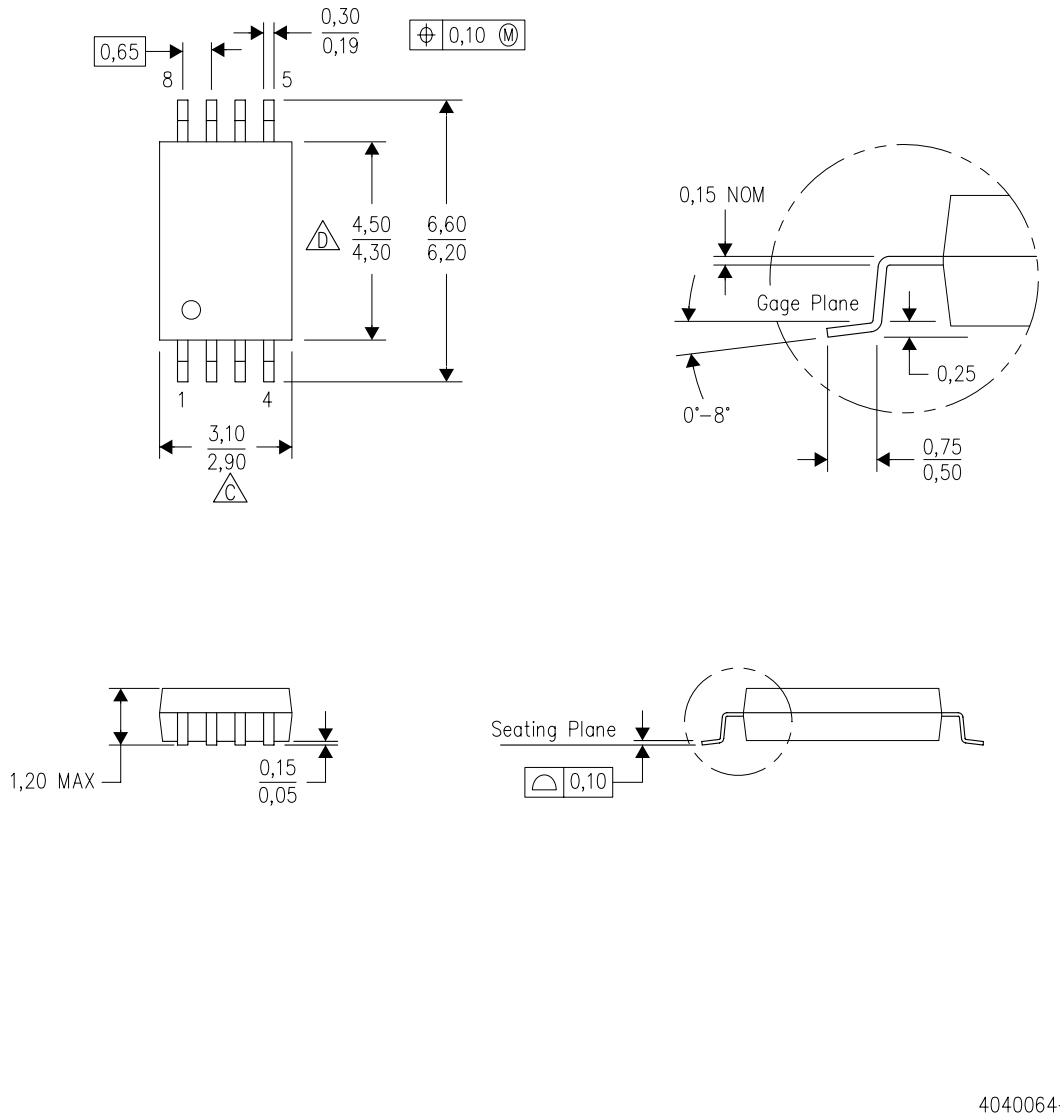
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G8) PLASTIC SMALL OUTLINE



4040064–2/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153